CLAIMS

What is claimed is:

1. A method of driving a non-volatile flip-flop circuit comprising;

a first inverter having an input terminal and an output terminal which are connected to a first memory node and a second memory node, respectively,

a second inverter having an input terminal and an output terminal which are connected to the second memory node and the first memory node, respectively,

a first pass transistor which has a gate connected to a word line and is connected between a first bit line and the first memory node,

a second pass transistor which has a gate connected to the word line and is connected between a second bit line and the second memory node,

a first switching element for control and a first variable resistor element which are connected serially to each other and are connected between the first memory node and a plate line, and

a second switching element for control and a second variable resistor element which are serially connected to each other and are connected between the second memory node and the plate line;

wherein the resistance values of the first and second variable resistor elements can be changed by the heat generated by a current;

the method comprising:

a STORE step and

a subsequent RECALL step,

the STORE step having

a first step in which both the first and second variable resistor elements are made low resistive, and

a second step which follows the first step, and in which while either the first or second variable resistor element, whichever is connected to the memory node storing "0", is maintained low resistive, only the variable resistor element which is connected to the memory node storing "1" is made high resistive, and,

in the RECALL step, "1" being set in the memory node which is connected to either the first or second variable resistor element, whichever is in a high resistive state, and "0" being set in the memory node which is connected to either the first or second variable resistor element, whichever is in a low resistive state.

2. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein the first step comprising, in the order stated below:

a step for placing the first and second switching elements for control in the ON state, while maintaining the state in which the supply voltage is applied to the power lines of the first and second inverters and the ground voltage is applied to the plate line,

a step for gradually increasing the voltage applied to the plate line from the ground voltage to a predetermined voltage, while maintaining the state in which the supply voltage is applied to the power lines of the first and second inverters, and the first and second switching elements for control are in the ON state,

a step for maintaining the voltage applied to the plate line at the predetermined voltage, while maintaining the state in which the supply voltage is applied to the power lines of the first and second inverters, and the first and second switching elements for control are in the ON state,

a step for gradually reducing the voltage applied to the plate line from the predetermined voltage to the ground voltage, while maintaining the state in which the supply voltage is applied to the power lines of the first and second inverters, and the first and second switching elements for control are in the ON state, and

a step for maintaining the state in which the

supply voltage is applied to the power lines of the first and second inverters, the ground voltage is applied to the plate line, and the first and second switching elements for control are in the ON state.

3. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein the second step comprising, in the order stated below:

a step for placing the first and second switching elements for control in the ON state, while maintaining the state in which the supply voltage is applied to the power lines of the first and second inverters and the ground voltage is applied to the plate line, and

a step for rapidly placing the first and second switching elements in the OFF state, while maintaining the state in which the supply voltage is applied to the power lines of the first and second inverters and the ground voltage is applied to the plate line.

4. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein the RECALL step comprising, in the order stated below:

a step for placing the first and second switching elements for control in the ON state, while

maintaining the state in which the ground voltage is applied to the power lines of the first and second inverters and the ground voltage is applied to the plate line,

a step for gradually increasing the voltage applied to the power lines of the first and second inverters from the ground voltage to the supply voltage, while maintaining the state in which the ground voltage is applied to the plate line and the first and second switching elements for control are in the ON state,

a step for placing the first and second switching elements for control in the OFF state, while maintaining the state in which the ground voltage is applied to the plate line and the voltage applied to the power lines of the first and second inverters is gradually increased to the supply voltage, and

a step for gradually increasing the voltage applied to the power lines of the first and second inverters and finally applying the supply voltage to the power lines of the first and second inverters, while maintaining the state in which the ground voltage is applied to the plate line and the first and second switching elements for control are in the OFF state.

5. A method of driving a non-volatile flip-flop

circuit according to claim 2, wherein the first and second switching elements for control are both transistors, and the voltage applied to the gate of the transistors is higher than the supply voltage.

6. A method of driving a non-volatile flip-flop circuit according to claim 3, wherein the first and second switching elements for control are both transistors, and the voltage applied to the gate of the transistors is higher than the supply voltage.

7. A method of driving a non-volatile flip-flop circuit according to claim 4, wherein the first and second switching element for control are both transistors and the voltage applied to the gate of the transistors is higher than the supply voltage.

8. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein

the first inverter comprises a first transistor and a second transistor complementing each other and each having a gate and a drain, the gates of the first and second transistors being connected to the first memory node and the drains of the first and second transistors being connected to the second memory node, and

the second inverter comprises a third transistor and a fourth transistor complementing each other and each having a gate and a drain, the gates of the third and fourth transistors being connected to the second memory node and the drains of the third and fourth transistors being connected to the first memory node.

9. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein the first and second inverters each comprises a MOS transistor and a resistor.

10. A method of driving a non-volatile flip-flop circuit according to claim 8, wherein

the first and third transistors are N-channel MOS transistors and

the second and fourth transistors are P-channel MOS transistors.

11. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein the first and second variable resistor elements each comprises a phase change material of a chalcogenide compound.

12. A method of driving a non-volatile flip-flop circuit according to claim 1, wherein each of the first

and second variable resistor elements has, in its high resistive state, a resistance value about 5 times as high as that in its low resistive state or higher.

13. A method of driving a non-volatile flip-flop circuit according to claim 8, wherein each of the first and second variable resistor elements has, in its high resistive state, a resistance value higher than the ON-resistance value of any of the first-fourth transistors.